WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor package comprising the steps of:

providing an elongated lead frame lying in a plane;

cupping a strap from the plane of the lead frame, thereby providing a nest in the lead frame;

inserting a semiconductor die in the nest so that a bottom surface of the semiconductor die is exposed for surface mounting connection; and

establishing electric contact between a top surface of the semiconductor die and an inner surface of the cupped strap.

2. The method defied in claim 1, further comprising the step of overmolding the lead frame with the semiconductor die with a plastic mold, thereby providing a housing which protects the lead frame and the semiconductor die.

3. The method defined in claim 1, wherein the semiconductor die is MOSFET whose top surface is the source electrode, the method further comprising the steps of attaching the top surface of the MOSFET to the inner surface of the cupped strap, and inverting the lead frame to provide a wire bond on the lead frame between the gate electrode of the MOSFET and a protrusion formed on the lead frame and extending into the nest after the semiconductor die has been mounted to the lead frame but before the overmolding of the lead frame.

4. The method defined in claim 2, further comprising the step of deflashing the molded lead frame.

5. The method defined in claim 2, further comprising the step of singulating the molded lead frame to form a plurality of frame segments each having

a respective cupped strap and a respective semiconductor device, thereby producing a multiplicity of individual semiconductor packages.